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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,100	02/09/2001	Aviv Malinovitch	P04729	6462

7590 10/07/2002

Docket Clerk
P.O. Drawer 800889
Dallas, TX 75380

EXAMINER
DEBERADINIS, ROBERT L

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/780,100	AVVIV MALINOVITCH et al.
Examiner	**Art Unit**
Robert L. DeBeradinis	2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 9, 2001*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-24* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Feb 9, 2001* is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,8,9,15,20 are rejected under 35 U.S.C. 102(b) as being anticipated by WEBSTER 6,195,755.

Regarding claims 1,8,20.

WEBSTER discloses for use in an integrated circuit of the type comprising at least two power supply domains (function circuits, column 4, line 7) in which each power supply domain comprises at least one module powered by the same voltage level, an apparatus for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode (column 5, lines 34-66, column 6, lines 1-50).

Regarding claims 2,9.

WEBSTER does not disclose a power sense cell.

WEBSTER discloses a variable power source (column 4, lines 43-45) having a control input terminal receiving an asserted logic state and a deasserted logic state for blocking an output signal to control a power management apparatus for integrated circuit application. The power sense cell is an inherent part of the variable power source control logic (refer to column 4, lines 5-45, column 5, lines 34-44).

Regarding claim 15.

WEBSTER discloses an integrated circuit of the type comprising at least two power supply domains (functional circuits) in which each power supply domain comprises at least one module powered by the same voltage level (column 5, lines 22-33), a method for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode (column 5, lines 35-44), said method comprising the steps of:

sensing with a power sense when said second power supply domain is in a low power mode; and

blocking said output signal in said first power supply domain from being sent to said second power supply domain when said power sense cell determines that said second power supply domain is in a low power mode (column 5, lines 35-44).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3,4,10,11,16,17,21,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over WEBSTER 6,195,755.

Regarding claims 3,4,10,11,16,17,21,22.

WEBSTER discloses functional circuits and a logical term, deasserted state, implying that a logical function has taken place (column 4, line 21).

WEBSTER does not disclose wherein said logic circuit comprises an and gate having as a first input said output signal of said first power supply domain, and having as a second input a signal from said power sense cell.

It would have been obvious to one having ordinary skill in the art at the time of this invention to arrange logic circuits that include AND gates to receive logic levels from a power sense cell to block signals and manage power to power supply domains on an integrated circuit to conserve power (column 4, lines 5-45, column 5, lines 34-45).

It would have been obvious to one having ordinary skill in the art at the time of this invention to sense power cells and to provide logic outputs from logic circuits that include AND gates, to control the power management apparatus of an integrated circuit.

Claims 5,6,7,12,13,14,18,19,23,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over WEBSTER 6,195,755 in view of SMALLEY 5,848,281.

Regarding claims 5,6,12,13,18,19,23,24.

WEBSTER discloses the apparatus as claimed in claim 2.

WEBSTER does not disclose a schmitt trigger.

SMALLEY discloses a schmitt trigger (column 7, lines 42-49) device operated as a synchronizer circuit for synchronizing the asynchronous sleep and idle signals with the clock signal.

It would have been obvious to one having ordinary skill in the art at the time of this invention to provide an apparatus as claimed in claim 2 wherein said power sense cell comprises a schmitt trigger circuit and an apparatus for synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from said power sense cell in order to maintain sensing transition to only occur during a clock transition to maintain system synchronization.

Regarding claims 7,14.

SMALLEY discloses power management including power control logic (figure 2) and D flip flops having a clock signal as an input and control signals from the power control logic (see figures 5A-6).

SMALLEY does not disclose:

a first D flip flop circuit having as one input a signal from said power sense cell, and having as a second input a clock signal;

a second D flip flop circuit having as one input an output signal from said D flip flop circuit and having as a second input said clock signal; and

an AND gate having as one input an output signal from said second D flip flop circuit, and having as a second input said clock signal.

It would have been obvious to one having ordinary skill in the art at the time of this invention to merely arrange D flip flops and logic gates to generate control signals to control a power management apparatus for integrated circuit applications.

Any inquiry concerning this communication should be directed to Robert L. DeBeradinis whose number is (703) 306-5857. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached on (703) 308-3119. The fax phone number for this Group is (703) 308-7722.

RLD

SEPTEMBER 26, 2002

BRIAN SIRCUS
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